Single Event Effects Induced on Atom Switch based Field Programmable Gate Array

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Abstract

Single event effects (SEEs) of atom switches (ASs) embedded on 40-nm complementary metal oxide semiconductor (CMOS) are investigated with both heavy ion and pulsed laser irradiation. In the evaluation of atom switch-based field programmable Gate Array (AS-FPGA), ASs show immunity against the irradiation and there is no change of the state of ASs both in a cross-bar switch and memory in look up tables (LUTs). It is supposed that ASs do not make any single event transients (SETs) noise when the ions hit. On the other hand, the CMOS layer shows SETs and new approaches to solve the SET in CMOS are proposed, especially for AS-FPGA application.

Introduction

Conventional field programmable gate array (FPGA)

- Anti-fuse-type
- SRAM-type
- Flash-type

✓ The atom switch FPGA (AS-FPGA) is another type of FPGAs which based on atom switch technology. 
✓ ASs are programmable conductive bridges electrically formed between two metals grown by electrochemical phenomenon.

Experimental setup

A. Sample preparation
✓ ASs are employed to FPGA as complimentary atom switch (CAS), in which the ASs are connected in series with the opposite direction.
✓ The CASs are used in LUTs, MUXs and cross-bar matrix in the logic tile of AS-FPGA.
✓ AS-FPGA composes of 44 by 48 programmable logic tiles and 4 by 48 RAM blocks array. The chip contains about 12.7 million of ASs.

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<th>Table 1 List of samples</th>
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<tr>
<td>Samples</td>
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<tr>
<td>AS-FPGA w/o D-FF</td>
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<tr>
<td>AS-FPGA w/ D-FF</td>
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<td>Hard-via-FPGA</td>
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B. Heavy ion irradiation

<table>
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<th>Table 2. Heavy ion test conditions</th>
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<tr>
<td>Net Energy</td>
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<tr>
<td>Ion</td>
</tr>
<tr>
<td>Xe</td>
</tr>
<tr>
<td>296</td>
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<tr>
<td>289</td>
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<td>197</td>
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C. Pulsed laser irradiation
✓ The wavelength and pulse duration are 1064 nm and 30 ps, respectively.
✓ The laser was irradiated via the backside of the chip which is composed of Si substrate.
✓ The full-width at half maximum (FWHM) of intensity is 4.2 μm with a 20x objective lens.

Results and Discussion

A. Heavy ion irradiation
✓ No state changing of ASs was observed up to 68.9 MeV/(mg/cm²) with 10⁷ particle/cm³ of ion fluences, with respect all samples.
✓ However, SETs were observed during both heavy ion and pulsed laser irradiation.
✓ Each SET cross-section (P SET /cm²/logic tile) is calculated by the following formula:

\[
\sigma_{SET} = \frac{\text{LET}}{1} \times \frac{1}{\text{SET intervals}} \times \frac{1}{\text{# of logic tiles}}
\]

B. Pulsed laser irradiation
✓ SETs were mainly captured from MUX and cross-bar matrix, as well as modules which are composed of unhardened CMOS logic such like transmission gates and selector transistors.
✓ In the cross-bar matrix, only set/reset transistors associated with ASs are used, which are I/O high voltage transistor.

SETs MITIGATION OUTLOOK

✓ The set/reset transistors with ASs may be responsible to the unexpectedly prolonged SETs.
✓ The transient noise was observed in the output when the duration of SET is more than 200 ps affected the timing of the logic tile as shown in Figure 5.

C. Pulsed laser irradiation
✓ The wavelength and pulse duration are 1064 nm and 30 ps, respectively.
✓ The laser was irradiated via the backside of the chip which is composed of Si substrate.
✓ The full-width at half maximum (FWHM) of intensity is 4.2 μm with a 20x objective lens.

Figure 3. (a) Box-and-whisker plot and histogram of SET cross-section in AS-FPGA w/o D-FF. (b) Histogram of SET pulse width distributions acquired in Xe irradiation with AS-FPGA w/o D-FF. Shaded area represents an unreliable region due to less sampling resolution.

Figure 4. Example result of pulsed laser irradiation test at 1000 pl. Box areas are scanned by laser and yellowish colored dots represent the points where SET occurred. The gray square is the area of the unit logic tile, while white lined squares are functional modules in the logic tile.

Figure 5. SPICE simulation results. The switch inserted in parallel with the set/reset transistor of AS was switched on for 100 to 1000 ps. The logic tile output voltage is plotted as a function of time. (1+)

Figure 6. SET mitigation examples for AS crossbar circuits.

✓ We proposed alternative circuits as shown in Figure 6 and conducted SPICE and semiconductor technology computer-aided design (TCAD) simulation to check those circuits for mitigating SETs:
(1) insertion of the series resistance to the set/reset transistor
(2) replacing the n-type transistor with p-type
(3) increasing on resistance of ASs.

AS-FPGA can control SET tolerance on the field since the resistance of ASs are tunable by programming.

Conclusion

ASs exhibited immunity to the state change up to 68.9 MeV/(mg/cm²), irrespective of the cell states. However, it was identified that the set/reset transistor was responsible to create the SETs unexpectedly prolonged. The possible techniques were discussed with simulations to utilize ASs in the space applications.

Acknowledgments

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Figure 2. (a) Illustration of the CAS-based memory cell which is used in LUT. (b) Illustration of the CAS-based routing MUX. (c) Schematic diagram of a unit logic tile.

Figure 7. SPICE simulation results of series resistance insertion. Transient noise became smaller when larger series resistance was inserted. (×)

Figure 8. TCAD mixed-mode simulation results of n-type and p-type transistor: (a) and (b) are simulation results of drain output voltage when 3, 5, 10, 40 MeV/(mg/cm²) ion hits on drain in n-type and p-type transistor, respectively.